

Serial No. 09,593,912
Attorney Docket No. E0897
Firm Reference No. AMDSP0368US

Reply to Office Action Dated July 21, 2004
Reply Dated October 21, 2004

REMARKS

Claims 1-18 and 27-34 are currently pending.

I. REJECTION OF CLAIMS UNDER 35 U.S.C. § 103

Claims 1-18 and 27-34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wong et al., U.S. Patent No. 5,809,026 ("Wong"), in view of Quigley et al., U.S. Patent No. 6,650,624 ("Quigley"). Withdrawal of the rejection is respectfully requested for at least the following reasons.

Wong discloses a multi-port network interface device including a transmit data bus; a receive data bus; a medium access controller (MAC) and a physical signaling (PLS) circuit. The PLS circuit is coupled to the transmit and receive data buses, and configured to interface to a network layer. Additionally, Wong discloses at least one transmitter is coupled to the transmit data bus and configured to transmit data to a physical layer. Wong further discloses at least one receiver is coupled to the receive data bus and configured to receive data from the physical layer. Wong also discloses the at least one receiver is configured to place data, received from the physical layer, on the receive data bus for transmission to the network layer by the MAC and PLS circuit; and the MAC and PLS circuit is configured to place data, received from the network layer, on the transmit data bus for transmission to the physical layer by the at least one transmitter. See, for example, the Abstract, Fig. 2, Col. 3, ln. 45 to Col. 5, ln. 60.

With regard to claims 1, 7, 13 and 16, the Examiner admits Wong does not disclose the following features:

Claim 1:

"logical circuitry to transmit a training sequence from the common bus port to the physical layer devices" and "the data block being transmitted in one of a number of time slots of a time division multiplexed transmission." See, for example, the Office action, page 4, lines 9-12.

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Claim 7:

"a memory coupled to the local interface;
operating logic stored on the memory and executable by the processor, the operating logic
further comprising:

logic to transmit a training sequence from the common bus port to the
physical layer devices; and

the data block being transmitted in one of a number of time slots of a time
division multiplexed (TDM) transmission." See, for example, the Office action, page 5,
lines 1-5.

Claim 13:

"means for transmitting a training sequence from the common bus port to the physical
layer devices;" and

"the data block being transmitted in one of a number of time slots of a time division
multiplexed (TDM) transmission."

Claim 16:

"transmitting a training sequence to the physical layer devices by way of a common bus,"
and

"the data block being transmitted in one of a number of time slots of a time division
multiplexed (TDM) transmission."

Accordingly, the Examiner contends Quigley discloses these features and that it would
have been obvious to one of ordinary skill in the art at the time of the invention to modify Wong
by using the features, as taught by Quigley, in order to provide an efficient and reliable
communication system. The Applicant respectfully disagrees.

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Claims 1, 7, 13 and 16 recite, *inter alia*, transmit(ing) a training sequence from the common bus port to the physical layer devices and the data block being transmitted in one of a number of time slots of a time division multiplexed (TDM) transmission. The training sequence is transmitted for an appropriate period of time that allows each of the physical layer devices 130 to identify its particular time slot. Thereafter, data is transmitted to the respective physical layer devices 130 through the appropriate time slots dedicated thereto. In this manner, a data block is transmitted from the MAC 120 to any particular physical layer device 130. See, for example, page 6, lns. 19-30 and FIGS. 3, 5A and 5B.

In contrast, Wong discloses a multi-port network interface device which provides a shared communication medium between equipment without the complexity or need for an external repeater. See, for example, Col. 1, lns. 55-67. Wong further discloses transmit data 36a is sent to every transceiver at the same time. Additionally, Wong discloses only one receiver may receive data at any one time since otherwise the received data would become garbled. See, for example, Col. 4, lns. 5-13 and lns. 28-31.

Therefore, even if Quigley discloses the features of a training sequence and a data block, there would not be motivation to modify Wong with the teachings of Quigley. That is, modifying Wong with the features of Quigley would defeat the use of Wong as a repeater. Wong is premised on transmitting data to every transceiver at the same time. One having ordinary skill in the art would not be motivated to destroy such operation by introducing a training sequence to enable transmitting data at different times as recited in the claimed inventions.

Therefore, since Wong alone or in combination with Quigley does not teach or suggest one or more of the features as claimed in claim 1, claims 2-6 and 27-29 that depend therefrom are believed to be in condition for allowance for at least the reasons stated above. Likewise, claim 7 and the claims that depend therefrom, i.e., claims 8-12 and 30-32, are patentable over Wong alone or in combination with Quigley. Similarly, claim 13 and the claims that depend therefrom, i.e., claims 14-15 and 33, are patentable over Wong alone or in combination with Quigley.

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Correspondingly, claim 16 and the claims that depend therefrom, i.e., claims 17-18 and 34, are patentable over Wong alone or in combination with Quigley.

II. CONCLUSION

In light of the foregoing, it is respectfully submitted that the present application is in condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in condition for allowance, the Examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present invention.

Any fee(s) resulting from this communication is hereby authorized to be charged to our Deposit Account No. 18-0988; Our Order No. E0897 (AMDSP0368US).

Respectfully submitted,
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